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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/665,884 | 09/20/2000 | Christopher H. Dick | X-501-1P US | 6804 |

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| EXAMINER | |
|---|---|
| PATHAK, SUDHANSHU C | |
| **ART UNIT** | **PAPER NUMBER** |
| 2634 | |

DATE MAILED: 02/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/665,884 | DICK ET AL. | |
| | Examiner | Art Unit | |
| | Sudhanshu C. Pathak | 2634 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *September 20th, 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4 and 6-17* is/are rejected.

7)☒ Claim(s) *2 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *September 20th, 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-to-17 are pending in the application.

### *Specification*

2. The abstract of the disclosure is objected to because:

Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.
Extensive mechanical and design details of apparatus should not be given.

Appropriate correction is required.

3. The disclosure is objected to because of the following informalities:

The "substitute" specification on Pg. 35-36 refers to a section called

"References", these should be listed in the submitted PTO-1449 Information

Disclosure Statement and not in the disclosure. .

Appropriate correction is required.

***Drawings***

4. Figures 1-to-16 should be designated by a legend such as "Prior Art" because only that which is known is illustrated, since these figures are only referred to in the "Background of the invention" in the Specification.

5. An element number should designate elements in each figure.

***Claim Objections***

6. Claim 4 is objected to because of the following informalities:

Claim 4 refers to "a first adder input" and also "a second adder input", furthermore, in Fig. 26 discloses multiple adders. Therefore, Claim 4 can be interpreted as describing an input of the multiple adders. It is recommended that this be changed to "a first input" and "a second input"

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 1, 3-4, 12-13 & 16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding to Claim 1, the claim refers to a DC-canceler comprising a sigma-delta modulator having the input terminal connected to the feedback-path input terminal and the sigma-delta output terminal connected to the feedback-path output terminal, however this is not what is described in the specification in Fig. 26, wherein the input terminal of the sigma-delta modulator is connected to the output terminal of a delay element and not the input terminal of feedback-path.

Regarding to Claim 3, the claim refers to a DC-canceler circuit further comprising a unit delay element having a delay-element input terminal connected to the feedback-path input terminal and a delay-element output terminal connected to the sigma-delta input terminal, however this is not what is described in the specification in Fig. 26, wherein the input terminal of the delay element is connected to the output terminal of a adder element and not the input terminal of feedback-path.

Regarding to Claim 4, the claim refers to a DC-canceler circuit further comprising an adder having a first input terminal connected the delay-element output terminal, a second input terminal connected to the feedback-path input terminal, however this is not what is described in the specification in Fig. 26, wherein the second input terminal of the adder is connected to the output terminal of the multiplier not the input terminal of feedback-path.

Regarding to Claim 12, the claim refers to a sigma-delta loop having a tunable center frequency comprising a tunable all pass network having an input terminal connected to the data input terminal, however this is not what is described in the

specification in Fig. 20, wherein the input terminal of the all pass network is connected to an adder.

Regarding to Claim 13, the claim refers to a sigma-delta loop having a tunable center frequency comprising a second tunable all pass network having an input terminal connected to the first all pass network output terminal, however this is not what is described in the specification in Fig. 20, wherein the input terminal of the all pass network is connected to another adder.

Regarding to Claim 16, the claim refers to a first adder having the first input connected to the output of the "second adder", the claim does not define a second adder therefore there is a lack of antecedent basis, further more freeing to Fig. 20 of the specification this should refer to a "second subtractor" which is also defined earlier.

***Claim Rejections - 35 USC § 102***

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 12-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Harris et al. (5,736,950).

Regarding to Claim 12, Harris discloses a sigma-delta loop having a tunable center frequency (Fig. 6), the loop comprising a data input terminal (Fig. 6, elements "X", "$X_o$"); a tunable all pass network (Fig. 6, element 113) having an input terminal of the all pass network is connected to an adder (Fig. 6, element 128); a global feedback network connected between the all pass network output terminal and the all pass network terminal input (Fig. 6, elements 113, 115, 120, 122, 124, 128); and

a local feedback network connected between the all pass network input and output terminals (Fig. 6, element 113, 116, 120, 122, 124, 128).

Regarding to Claim 13, Harris discloses a sigma-delta loop having a tunable center frequency as described above. Harris discloses the loop further comprising a second tunable all-pass network (Fig. 6, element 115) having an input terminal connected to an adder, which is further, connected to the output of the first all pass, network (Fig. 6, elements 113-115); and an output terminal.

Regarding to Claim 14, Harris discloses a sigma-delta loop having a tunable center frequency as described above. Harris further discloses the global feedback comprising a first co-efficient multiplier connected between the first all pass network output and input terminals (Fig. 6, element 116), and a second co-efficient multiplier connected between the output terminal of the second all pass network and the input of the first all pass network (Fig. 6, element 118).

Regarding to Claim 15, Harris discloses a sigma-delta loop having a tunable center frequency as described above. Harris further discloses the loop comprising a quantizer having the input connected to the global feedback network and the output connected to the first all pass network input terminal (Fig. 6, element 122).

Regarding to Claim 16, Harris discloses a tunable sigma-delta loop comprising a data input terminal (Fig. 6, element "X") to receive data; a first subtractor (Fig. 6, element 124) having a first, second input terminals and an output terminal; a second subtractor (Fig. 6, element 128) having a first input terminal connected to the output of the first subtractor, a second input terminals and an output terminal; a first adder

having a first input terminal connected to the output of the second subtractor (Fig. 1, elements 128, 113), a second input terminal and an output terminal; a tunable app-pass network having the input connected to the output of the first adder and the output terminal connected to the second input of the first adder (Fig. 6, element 113); a local feedback having the input connected to output of the all pass network and output connected to second input of the second subtractor (Fig. 6, element 126); a global feedback having the input connected to output of the all-pass output and global feedback output terminal (Fig. 6, elements 113, 116, 120, 122, 124, 128); and a quantizer having a quantizer input terminal connected to the global-feedback output terminal and a quantizer output terminal connected to the second input terminal of the first subtractor (Fig. 6, element 122).

Regarding to Claim 17, Harris discloses a sigma-delta loop having a tunable center frequency as described above. Harris further discloses the loop comprising a second adder having a first adder input terminal connected to the first-mentioned all-pass network output terminal, a second adder input terminal, and an adder output terminal connected to the local-feedback input terminal (Fig. 6, element 115, 126); a second tunable all-pass network having an all pass network input terminal connected to the output terminal of the second adder and a all-pass network output terminal connected to the second input terminal of the second adder (Fig. 7, element 115); a second global feedback network having a global feedback input terminal connected to the all-pass network output terminal of the second all-pass network and a global-feedback output terminal (Fig. 6, element 115, 118, 120); a third adder

having a first input terminal connected to the global-feedback output terminal of the first-mentioned global feedback network, a second input terminal connected to the output of the second global feedback network and output terminal connected to the input of the quantizer (Fig. 6, element 120, 122)

***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 6, 10 & 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over M.E. Frerking (Digital Signal Processing in Communications Systems; Published by Van Nostrand Reinhold; Copyright 1994; Pg. 124-128) in view of Harris et al. (Configurable Logic for Digital Communications: Some Signal Processing Perspectives; IEEE Communications Magazine; August 1999; Pg. 107-111).

Regarding to Claim 6, 10 & 11, Frerking discloses a receiver with digital signal processing (Fig. 4.16, Pg. 125 & Fig. 4.15 & Frequency Translation, Pg. 124, lines 18-27 & Pg. 125, lines 1-5). However, Frerking does not discloses a digital signal processing chip configured to include a data input / output ports and a sigma-delta modulator.

Harris discloses a FPGA (field programmable gate array) chip for performing signal processing algorithms on data received by a communications receiver (Pg.

107, Column 1, lines 15-53 & Fig. 1-2 & Pg. 108, Column 1, lines 1-12, 25-26 & Pg. 111, Column 1, lines 22-35, 47-63). Harris further discloses the chip comprising a sigma-delta modulator connected to the input port of the chip and having a control signal output port (Fig. 1-2 & Pg. 108, Column 1, lines 25-26 & Pg. 108, Column 2, lines 1-25 & Pg. 109, Column 1, lines 1-47). Harris also discloses a feedback path connected between the control signal output port and the data input port (Fig. 1-2). Furthermore, Harris discloses the processing chip to be a FPGA, which is a programmable logic device. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that implementing the FPGA chip as a digital receiver as described in Harris into the communications receiver as described in Frerking to perform the signal processing functions on the signal received improves the accuracy of the signal processing while maintaining the flexibility provided by the software based solutions thus satisfying the limitations of the claims.

11. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over M.E. Frerking (Digital Signal Processing in Communications Systems; Published by Van Nostrand Reinhold; Copyright 1994; Pg. 124-128) in view of Harris et al. (Configurable Logic for Digital Communications: Some Signal Processing Perspectives; IEEE Communications Magazine; August 1999; Pg. 107-111) in further view of Harris et al. (5,736,950) in further view of Sutterlin et al. (5,471,209).

Regarding to Claim 7, Frerking in view of Harris discloses a receiver comprising a sigma-delta modulator as described above. However, Frerking in view of Harris does not disclose the feedback path to include an analog filter.

Harris discloses a sigma-delta modulator implemented in a receiver with multiple signal processing applications (Abstract, lines 10-18 & Fig. 1-2). Harris further discloses the sigma-delta modulator comprising a digital-to-analog (D/A) in the feedback loop when in an analog-to-digital (A/D) configuration, so as to compare analog input and analog feedback signals (Fig. 1, element 29 & Fig. 2, element 129 & Column 4, lines 16-23). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Harris teaches that implementing the sigma-delta modulator in an A/D configuration requires implementing a D/A converter in the feedback loop so as to compare the input and feedback signals in the receiver as described in Frerking in view of Harris. However, Frerking in view of Harris in further view of Harris does not disclose implementing an analog filter in the feedback loop of the sigma-delta modulator.

Sutterlin discloses a sigma-delta converter comprising an analog filter connected between the feedback signal output port and the filter input terminal (Fig. 2a-b & Column 2, lines 9-16). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that implementing the filter as described in Sutterlin in the feedback path after the D/A converter as described in Frerking in view of Harris in further view of Harris would smooth out the analog signal so as to

more accurately compare the incoming analog signal with the feedback analog signal for better performance of the digital receiver performance.

12. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over M.E. Frerking (Digital Signal Processing in Communications Systems; Published by Van Nostrand Reinhold; Copyright 1994; Pg. 124-128) in view of Harris et al. (Configurable Logic for Digital Communications: Some Signal Processing Perspectives; IEEE Communications Magazine; August 1999; Pg. 107-111) in further view of Harris et al. (5,736,950) in further view of Sutterlin et al. (5,471,209) in further view of Velez et al. (6,289,044).

Regarding to Claim 8, Frerking in view of Harris in further view of Harris in further view of Sutterlin discloses a receiver comprising a sigma-delta modulator as described above. However the above-mentioned references do no disclose an automatic gain control circuit in the receiver feedback path.

Velez discloses an automatic gain control circuit (AGC) implemented in conjunction with an analog-to-digital (A/D) converter (Fig. 1, elements 14, 16). Furthermore Velez discloses the A/D converter implemented as a sigma-delta modulator (Fig. 2). Velez also discloses that the analog component to be an AGC (Fig. 2, element 14 & Column 1, lines 30-43 & Column 2, lines 45-67) and the AGC control signal provided by the feedback path through the AGC control signal circuit (Fig. 1, element 24 & Column 1, lines 30-43 & Column 2, lines 45-67). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Velez teaches that it is possible to implement an AGC circuit in the receiver to

provide the input for the A/D converter with the control signal for the AGC circuit provided by the feedback loop from the output of the ADC converter as implemented by a sigma-delta modulator in the receiver as described in Frerking in view of Harris in further view of Harris in further view of Sutterlin so as to exploit the complete dynamic range of the ADC.

13. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over M.E. Frerking (Digital Signal Processing in Communications Systems; Published by Van Nostrand Reinhold; Copyright 1994; Pg. 124-128) in view of Harris et al. (Configurable Logic for Digital Communications: Some Signal Processing Perspectives; IEEE Communications Magazine; August 1999; Pg. 107-111) in further view of Harris et al. (5,736,950) in further view of Sutterlin et al. (5,471,209) in further view of Hein et al. (6,104,794).

Regarding to Claim 9, Frerking in view of Harris in further view of Harris in further view of Sutterlin discloses a receiver comprising a sigma-delta modulator as described above. However the above-mentioned references do no disclose a voltage controlled oscillator circuit in the receiver feedback path.

Hein discloses a voltage controlled oscillator circuit (VCO) implemented in conjunction with a sigma-delta modulator analog-to-digital (A/D) converter (Fig. 2, elements 201, 202 & Fig. 3b & Fig. 5, element 535). Hein further discloses the oscillator to provide a clock for the sigma-delta A/D converter (Column 8, lines 44-65 & Column 10, lines 19-40). Hein also discloses the oscillator to be implemented as a phase lock loop comprising a voltage controlled oscillator (Fig. 5 & Column 12,

lines 51-67). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Hein teach that the sampling clock implemented in a sigma-delta modulator A/D converter as described in Frerking in view of Harris in further view of Harris in further view of Sutterlin using a voltage controlled oscillator wherein the control signals provided in the feedback loop.

***Allowable Subject Matter***

14. Claims 2 & 5 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sudhanshu C. Pathak whose telephone number is (703)-305-0341. The examiner can normally be reached (Monday-Friday) from 8:30 AM to 5:30PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin, can be reached at: (703) 305-4714. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
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Or faxed to: (703) 872-9314 (for Technology Center 2600 only)
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